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Comparative Analysis of 7T and 6T SRAM Using 0.18µm Technology

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1. Abstract

Modern technology is spreading with a very fast rate and time to market is very less, the parameter which is greatest today becomes worst tomorrow. Significant notice has been paid to the design of low-power, high-performance fast responding SRAMs (Static Random Access Memories), since they are a critical component in both hand-held devices and high-performance processors. A key in improving the performance of the system is to use an optimum sized SRAM.

In this research work, an SRAM compiler has been developed for the automatic layout of memory elements in the ASIC environment by using tools like MICRO WIND or using CADENCE. The compiler generates an SRAM layout based on a given SRAM size, input by the user, with the option of choosing between fast vs. low-power SRAM and other desired parameter as well. The best way to obtain desired implementation of developed logic by precise control over parameter along with optimization of circuit like Array partitioning is used to partition the SRAM into blocks in order to reduce the total power consumption, using thin wire, effective contact, and metal to metal contact. In this work, we discuss the implementation of the SRAM for comparative analysis mainly we are concern about 6T and 7T SRAM cell analysis. Further, we demonstrate that there is a tradeoff between optimizing the leakage power and improving the immunity to yielding error and synthesis results indicating the estimated area and delay

2. Keywords

Low Power, SRAM, Stand Alone Devices, Negative Word Line, 4T SRAM, 6T SRAM, 7T SRAM Load Less, Word Line.

3. Introduction

Yielding errors or transient errors are circuit errors caused due to excess charge carriers induced primarily by external radiations due less control over isolation parameter. Radiation directly or indirectly induces a localized ionization capable of upsetting internal data states and sometimes allows metal migration as well but this possibility is very-very less. While these errors cause a displease event, the circuit itself is not damaged. These errors are particularly upsetting for memory elements as the stored values of the bits are changed and in digital everything is in binary zero ,one means change in single bit causes discarding, resore or correction of whole data in that particular cycle of instruction execution as well . The frequency of yielding errors in SRAM memories is becoming a critical issue as technology continues to shrink [1, 2, and 3] because everything is going towards compactness like micro fluid tech. Specifically, yielding errors in SRAM memories can be catastrophic in applications such as networking equipment because a bit flip can result in information packets this can be better understand by money transfers sent to the wrong account. Trends such as smaller supply voltages and reduced capacitive values at the nodes and parasitic formation with technology scaling are potential concerns for the memory cell's susceptibility to yielding errors [4].

There is important term which is tradeoff between different parameter like threshold voltage, supply voltage, leakage current, gain, latency, power dissipation. Another major concern in future SRAMs is the leakage power consumption. Due to the reduced threshold voltage in future technologies, leakage power is increasing rapidly. As most of the current processors employ large on-chip memories for resources such as instruction and data caches, translation look aside buffers and prediction tables, controlling leakage in memories is important [5].

Yielding errors from alpha particles were first reported by May and Woods [4]. Since then significant attempt has been spent in dealing with transient errors. A significant source of ionizing radiation in devices is from alpha particles from the naturally occurring radioactive impurities in device materials. Alpha particles are one of the many radiations that can be emitted when the nucleus of an unstable isotope decays to a lower energy state [5].

Power SRAMs have become a critical component of many VLSI chips. This is especially true for microprocessors, where the on-chip cache sizes are growing with each generation to bridge the increasing divergence in the speeds of the processor and the main memory this logic mostly uses in system on

chip. The power dissipation has become an important consideration due to the increased integration, operating speeds and the explosive growth of battery operated appliances. The leakage current of the memory will be increased with the capacity such that more power will be consumed even in the standby mode. The existing SRAM cells can be divided into two groups in terms of transistor numbers: standard six-transistor (6T) shown in Figure 1, seven-transistor (7T) Figure 3, and four-transistor (4T) SRAM Figure 2 with resistive load. In a 6T SRAM cell, the transistors connected to the bit lines are called access transistors.

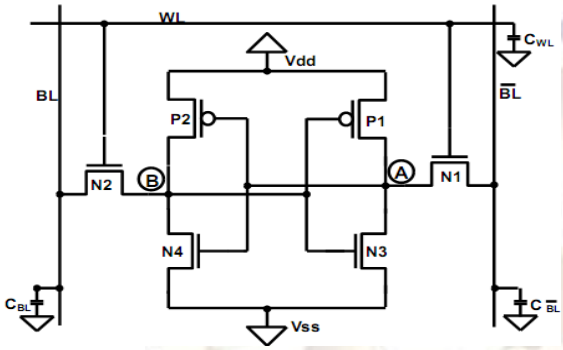


Fig.1 Schematic for a 6T SRAM cell

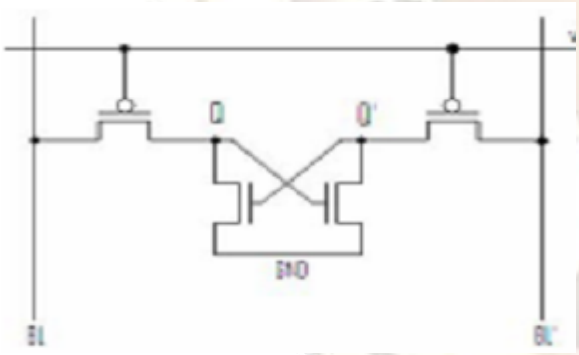


Fig. 2: Schematic of a load less 4T SRAM cell

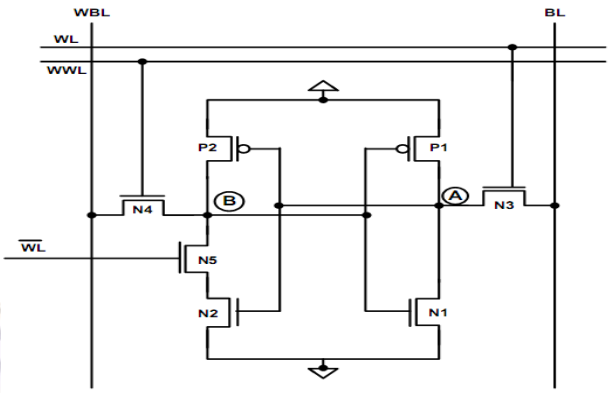


Fig.3 schematic for a 7T SRAM cell

The transistors pull the cell values (Q and Q') to V_{DD} are called load transistor, and the ones connected to ground are called driver transistors. The traditional 4T-SRAM with two load resistors instead of two load transistors dominates the standalone SRAM market since they have much less cell area than 6T-SRAM cells. A pair of PMOS transfer transistors is used to store and retain full-swing signals in the cell without a refresh cycle. The memory cell size is 35% smaller than a 6T cell using the same design rule with CMOS 0.18 micron technology.

4. Design and Implementation:

Low-power design in this work, we suggest a NWL scheme using which we reduce the leakage current of the access transistors in the standby mode. A current mode sense-amplifier is also employed to nullify the loss of the access speed. The proposed SRAM design is carried out by a typical CMOS technology (Taiwan Semiconductor Manufacturing Company) such that it is fully compatible with CMOS digital design. Also we propose here a new load less 4T SRAM cell in which we are using NMOS transistors as pass transistors and PMOS transistors as latch transistors because PMOS transistors exhibits smaller leakage current than the NMOS transistors as described in the next section. We gave the name "NPPL" (N pass P latch) to this SRAM.

As compared to the 6T SRAM cell and 7T SRAM cell, a loadless 4-T SRAM cell size is 35% to 45% smaller and also the power consumption of the loadless 4–T SRAM cell using µm like .18µm CMOS technology. Hence the loadless 4-T SRAM cell is widely used in microprocessor as embedded cache. For saving the power and reduce the cell area we propose 4-T SRAM cell to construct the SRAM memory. The major goal of this design is to decrease the standby current of inactive cells i.e., the leakage current of the cell pass

transistors. There is most important thing is tradeoff between parameter.

Leakage current of NB and NWL schemes: From the following equation we can formulate the

$$V_{TH} = V_{THO} + \gamma \left(\sqrt{|2\emptyset F| + V_{SB}} - \sqrt{2\emptyset F}\right)$$

Where V_{THO} represents the threshold voltage with a zero substrate voltage, $\emptyset_F$ is electrostatic potential, γ is the body coefficient and V_{SB} is the substrate voltage. According to this formula applying a negative voltage to the bulk of NMOS or a positive voltage to the that of PMOS V_{TH} will be increased therefore the leakage current will also be decreased. Fig. 4.1(a) and4.1 (b) shows the schematic and simulation of the leakage current in NWL scheme respectively. Fig. 4.2 and 4.3 shows the schematic and simulation result for the NB line scheme respectively. Simulation result shows that the V_{WL} and V_{bulk} are varied from -1.5 To 0 V, V_{dd} =1.9V.it is found that the leakage current of NWL scheme is smaller than that of the NB scheme. The NB line scheme needs a stable bias at -0.6 V while the NWL schemes only needs the bias below -0.3 V. it is also found that the leakage current of both the schemes decrease with the increase in more negative voltage. Also for the NB scheme a triple well structure is required to isolate the well voltage of the transistor. It is one of the reasons due to which we are using here the NWL scheme.

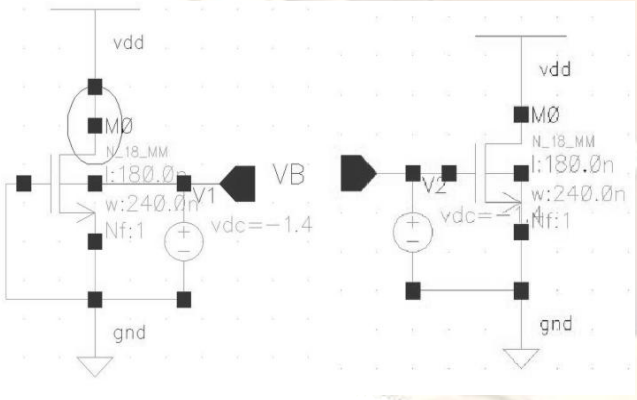


Fig. 3.1(a) and3.1 (b) Simulation circuits of the NB and NWL schemes.

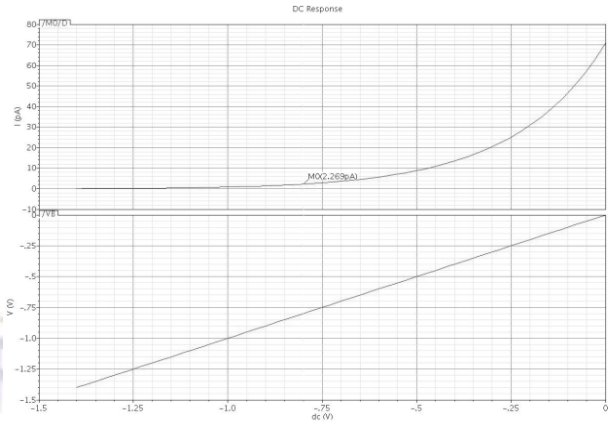


Fig.3.2 leakage current of the NB line scheme.

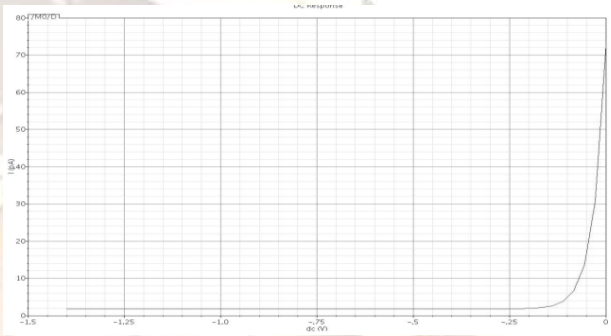


Fig.3.3 reduced leakage current of the NWL scheme.

The seven transistors memory cell is designed by adding a data protection NMOS Transistor N5 between node B and transistor N2 [1]. While SRAM cell is being accessed, WL is in activated state, 0 and N5 is OFF. Since N5 prevents the volt age at Node B From decreasing, the data bit is not reserved even if Node A voltage greatly exceeds Shown in Figure 3 Seven transistor SRAM consists of three word lines which are WWL, $\overline{WL}$, WL and two complementary bit lines BL and WBL. $\overline{WL}$ and WL are complementary and $\overline{WL}$ is Used to control the word lines WWL and WL. The write operation for SRAM 7T is same as that of 6T SRAM cell. In write operation one of the bit line is charged and the other discharged and the word lines WWL and WL are closed in order to write in the nodes A and B. During data retention period, when the SRAM cell is not being accessed, word line signal WL is 1 and NMOS transistor N5 is ON. The use of two CMOS inverters results in high cell stability. During read operation, the logical threshold voltage of the CMOS inverter driving node B increases greatly when the data protection NMOS transistor N5 is turned off. For this re as on, the re ad value at A = 0 remains large even when access NMOS transistor N3 is turned on and node A voltage increases.

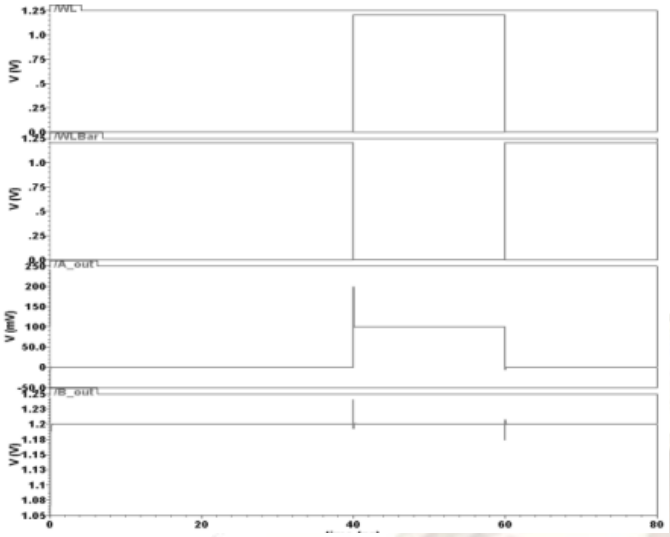
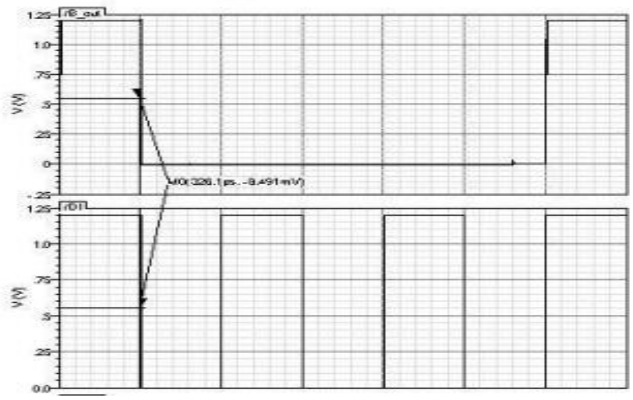


Fig.4 showing the results for 7T SRAM cell

The voltage dividing effect takes place at the inverter which stores 0, will be pulled up. In order to stop this transition the 7th transistor at the other node is turned off so that the node which stores 1 will not be pulled down b y the driver transistor as it acts a switch between the node and the driver transistor. In read operation the SRAM cell is isolated from the bit lines and the bit lines are precharged to V_{DD}. When the word lines are closed the bit lines which is connected to the node which stores 0 will be discharged through pass transistor while the other bit line stays high as shown in Figure 4.Simulation Waveforms for 6T SRAM cell and 7T SRAM cell Figure 5 and 6, respectively for write and read operation in 6T SRAM cell when we writing zero, and Figure 7 and 8



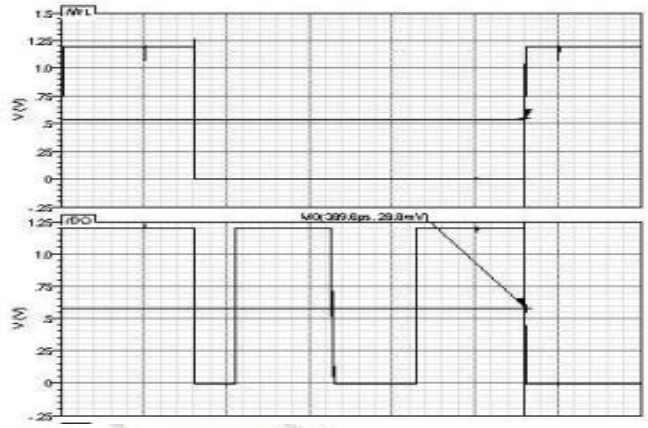


Fig.5

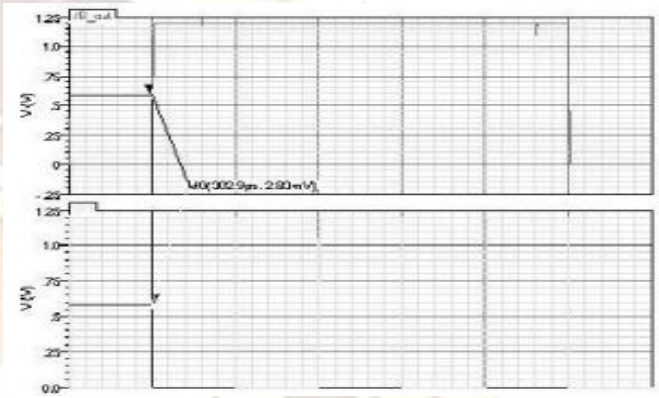


Fig.6

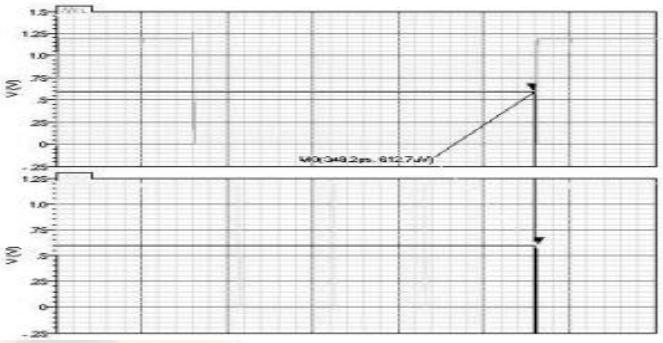


Fig.7

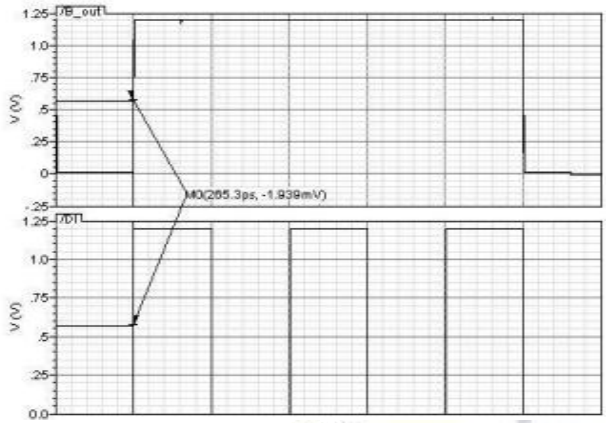


Fig.8

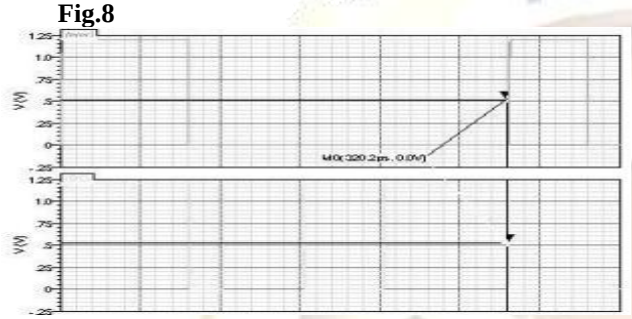


Fig.9

The synthesis results can be better analyzed by tabular representation.

	Write Operation	Delay (ps)	Read operation	Delay (ps)
SRAM 6T	W rite 0	330	Read 0	389.5
SRAM 7T		260		350.7
SRAM 6T	W rite 1	330	Read 1	380.3
SRAM 7T		270		263.5

Table3.1
Static noise response

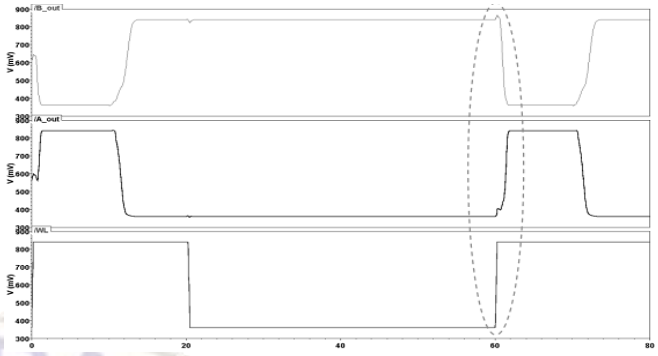


Fig.10

Voltages		SRAM 6T	SRAM 7T
V_{DD}	V_{ss}	Read Delay (ps)	Read Delay (ps)
1.08	0	16.3	10.22
1.08	0.12	25.94	15.36
0.96	0.12	47.65	27.62
0.96	0.24	55.68	33.02
0.84	0.24	64.13	58.53
0.84	0.36	78.24	68.36
0.72	0.36	89.98	80.4
1.2	0	10.5	5.6

Table3.2

Though 7T SRAM can perform better than 6T at low V_{DD} it has limiting factors:

1. The Table 3.2 shows the comparison is made till V_{DD} = 0.72v and V_{SS}= 0.36v-:
These are the maximum low voltages that this 7T SRAM can perform according To the transistor sizing. If we operate 7T SRAM lower than the stipulated voltage Levels then the write operation cannot be performed, since the write margin Decreases with decreasing $V_{DD.}$

2. Read operation at low-V_{DD}-:
Levels result in storage data destruction in SRAM cells this is due to the leakage current of PMOS transistor P2. This is shown in Figures as the 6T SRAM cell is operated at low $V_{DD.}$

5. Conclusion and Future application:

A Comparative Analysis of 4T, 7T and 6T SRAM With an optimized area which allows precise control over power and speed is presented. The effect of optimizing on the area and speed has been examined experimentally. The design has been mapped and optimized on tools like Micro wind, Cadence. The presented Comparative Analysis of 4T, 7T and 6T SRAM

run at slightly faster clock speed with used area less than that used previously. This logic should be mapped into next generation of microelectronics which is micro fluid chips.

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