Fault Tolerance in bit swapping LFSR using FPGA Architecture

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ABSTRACT

The design for low power has become one of the greatest challenges in high-performance very large scale integration (VLSI) design. It has been found that the power consumed during test mode operation is often much higher than during normal mode operation. This is because most of the consumed power results from the switching activity in the nodes of the circuit under test (CUT), which is much higher during test mode than during normal mode operation. BIST is a design technique that allows a circuit to test itself. In this, the test performance achieved with the implementation of BIST is proven to be adequate to offset the disincentive of the hardware overhead produced by the additional BIST circuit. The technique can provide shorter test time compared to an externally applied test and allows the use of low-cost test equipment during all stages of production. BIST technique uses linear feedback shift register (LFSR) for generating test pattern. The proposed design, called bit-swapping LFSR (BS-LFSR), is composed of an LFSR and a 2 × 1 multiplexer. When used to generate test patterns for scan-based built-in self-tests, it reduces the number of transitions that occur at the scan-chain input during scan shift operation by 50% when compared to those patterns produced by a conventional LFSR. Hence, it reduces the overall switching activity in the circuit under test during test applications. The BS-LFSR is combined with a scan-chain-ordering algorithm that orders the cells in a way that reduces the average and peak power (scan and capture) in the test cycle or while scanning out a response to a signature analyzer. These techniques have a substantial effect on average- and peak-power reductions with negligible effect on fault coverage or test application time.

Keywords: FPGA, Fault Tolerance, LFSR, BIST.

1. INTRODUCTION

Technology provides smaller, faster and lower energy devices which allow more powerful and compact circuitry, however, these benefits come with cost-the nano scale devices may be less reliable, thermal-and shot- noise estimations alone suggest that the fault rate of an individual nanoscale device may be orders of magnitude higher than today's devices. As a result, we can expect combinational logic be susceptible to faults. So in order to test any circuit or device we require separate testing technique which should be done automatically, for that purpose we are going to BIST.Reduce the power consumption in scan-based built-in self-tests (BISTs) is by using scan chain-ordering techniques. The bit-swapping LFSR (BS-LFSR), is composed of an LFSR and a 2 × 1multiplexer. When used to generate test patterns for scan-based built-in self-tests, it reduces the number of transitions**.** The proposed BS-LFSR generates the same number of 1s and 0s at the output of multiplexers after swapping of two adjacent cells; hence, the probabilities of having a 0 or 1 at a certain cell of the scan chain before applying the test vectors are equal. Hence, the proposed design retains an important feature of any random TPG. In the BS-LFSR, consider the case that $c1$ will be swapped with $c2$ and $c3$ with $c4, \ldots, cn-2$ with $cn-1$ according to the value of cn which is connected to the selection line of the multiplexers. In this case, we have the same exhaustive set of test vectors as would be generated by the conventional LFSR, but their order will be different and the overall transitions in the primary inputs of the CUT will be reduced. VLSI technology progress for finer dimension and larger chip area has lead to more complex process and introduction of new and more complex material system. Due to higher defect density and complicated fabrication technique the cost of manufacturing has increased. The increase in defect/fault complexity factor has lead to more devices being effective and hence reduced the yield. Researches for improving yield using various techniques are being carried out since many years. One of the ways to achieve higher yield is use of fault tolerance.

2. Built-In Self-Test (BIST)

BIST is a viable approach to test today's digital systems. With the ever increasing need for system integration, the trend today is to include in the same VLSI device a large number of functional blocks, and to package such devices, often, in Multi-Chip Modules (MCMs) that comprise complex systems. This leads to difficult testing problems in the manufacturing process and in the field**.** An attractive approach to solve these problems is to use a multi-level integrated Built-In Self-Test (BIST) strategy**.**

3. Linear feedback shift register (LFSR)

Linear feedback shift registers (LFSRs) are commonly used as test pattern generators (TPGs) in low overhead built-in self-test (BIST) schemes. This is due to the fact that an LFSR can be built with little area overhead. Attainment of high fault coverage with sequences of practical lengths has traditionally been the main objective of BIST techniques. Even though this still remains the main objective, we believe, reducing heat dissipated during test application is becoming another important objective.

EXISTING:

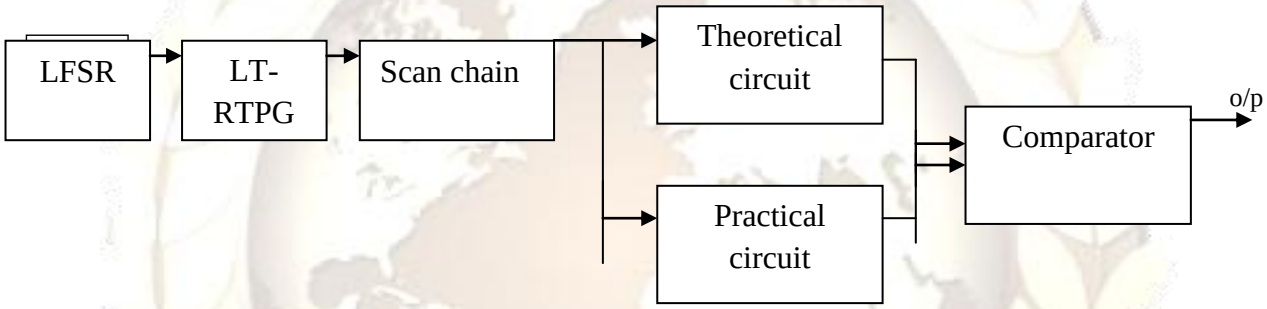

Figure 1.External L.F.S.R

The above figure shows the external LFSR by using bit swapping technique. Bit swapping is a swap of a bit from ‘m’ position to tone ‘n’ position. It is used to reduce the transitions occurred at the input side of applying test vectors to circuit. The proposed BS-LFSR reduces the average and instantaneous weighted switching activity (WSA) during test operation by reducing the number of transitions in the scan input of the CUT. So from the above circuitry we can reduce the peak power while applying the test vectors to the circuitry. By reducing the number of transitions in the L.F.S.R we are going to reduce the peak power.

4 .BIT SWAPPING LFSR

From this BIT SWAPPING technology we are going to reduce the peak power. By connecting multiplexers on the LFSR register as shown in above arrangement the number of transitions are decreased for that cell which are under bit swapping. The below table shows the number of transitions in each register in LFSR without applying BIT SWAPPING technology, after applying bit swapping technology. Two cells in an n-bit LFSR are considered to be adjacent if the output of one cell feeds the input of the second directly (i.e., without an intervening XOR gate). Each cell in a maximal-length n-stage LFSR (internal or external) will produce a number of transitions equal to $2n-1$ after going through a sequence of $2n$ clock cycles. The sequence of 1s and 0s that is followed by one bit position of a maximal-length LFSR is commonly referred to as an m sequence. Each bit within the LFSR will follow the same m-sequence with a one-time-step delay. The m-sequence generated by an LFSR of length n has a periodicity of $2n - 1$. It is a well-known standard property of an m-sequence of length n that the total number of runs of consecutive occurrences of the same binary digit is $2n-1$.The beginning of each run is marked by a transition between 0 and 1; Therefore, the total number of transitions for each stage of the LFSR is $2n-1$. This lemma can be proved by using

the toggle property of the XOR gates used in the feedback of the LFSR. Consider a maximal-length *n*-stage internal or external LFSR ($n > 2$). We choose one of the cells and swap its value with its adjacent cell if the current value of a third cell in the LFSR is 0 (or 1) and leave the cells un swapped if the third cell has a value of 1 (or 0). Fig. 1 shows this arrangement for an external LFSR (the same is valid for an internal LFSR). In this arrangement, the output of the two cells will have its transition count reduced by T saved = $2(n-2)$ transitions. Since the two cells originally produce $2 \times 2n-1$ transitions, then the resulting percentage saving is *Saved*% = 25%. The total percentage of transition savings after n swapping is 25%. In the case where cell *x* is not directly linked to cell *m* or cell *m*+ 1 through an XOR gate, each of the cells has the same share of savings (i.e., 25%). show the special cases where the cell that drives the selection line is linked to one of the swapped cells through an XOR gate. In these configurations, a single cell can save 50% transitions that were originally produced by an LFSR cell. Lemma 3 and its proof are given; other lemmas can be proved in the same way. For an external *n*-bit maximal-length LFSR that implements the prime polynomial $xn + x + 1$ as shown in Fig. 2, if the first two cells ($c1$ and $c2$) have been chosen for swapping and cell *n* as a selection line, then $o2$ (the output of MUX2) will produce a total transition savings of $2n-2$ compared to the number of transitions produced by each LFSR cell, while $o1$ has no savings (i.e., the savings in transitions is concentrated in one multiplexer output, which means that $o2$ will save 50% of the original transitions produced by each LFSR cell).There are eight possible combinations for the initial state of the cells $c1$, $c2$, and *cn*. If we then consider all possible values of the following state, we have two possible combinations (not eight, because the value of $c2$ in the next state is determined by the value of $c1$ in the present state; also, the value of $c1$ in the next state is determined by "$c1$ xor *cn*" in the present state). Table I shows all possible and subsequent states. It is important to note that the overall savings of 25% is not equally distributed between the outputs of the multiplexers. This is because the value of $c1$ in the present state will affect the value of $c2$ and its own value in the next state ($c2$(Next) = $c1$ and$c1$(Next) = "$c1$ xor *cn*"). To see the effect of each cell in transition savings, Table I shows that $o1$ will save one transition when moving from state (0,0,1) to (1,0,0), from (0,1,1) to (1,0,0), from (1,0,1) to(0,1,0), or from (1,1,1) to (0,1,0). In the same time, $o1$ will increase one transition when moving from (0,1,0) to (0,0,0), from (0,1,0) to (0,0,1), from (1,0,0) to (1,1,0), or from (1,0,0) to (1,1,1). Since $o1$ increases the transitions in four possible scenarios and save transitions in other four scenarios, then it has a neutral overall effect because all the scenarios have the same probabilities. For $o2$, one transition is saved when moving from (0,1,0) to(0,0,0), from (0,1,0) to (0,0,1), from (0,1,1) to (1,0,0), from (1,0,0) to(1,1,0), from (1,0,0) to (1,1,1), or from (1,0,1) to (0,1,0). At the same time, one additional transition is incurred when moving from state(0,0,1) to (1,0,0) or from (1,1,1) to (0,1,0). This gives $o2$ an overall saving of one transition in four possible scenarios where the initial states has a probability of 1/8 and the final states of probability 1/2;hence, *P*save is given by *P*save = $1/8 \times 1/2 + 1/8 \times 1/2 + 1/8 \times 1/2 + 1/8 \times 1/2 = 1/4$. If the LFSR is allowed to move through a complete cycle of $2n$states, then Lemma 1 shows that the number of transitions expected to occur in the cell under consideration is $2n-1$. Using the swapping approach, in 1/4 of the cases, a saving of one transition will occur, giving a total saving of $1/4 \times 2n = 2n-2$. Dividing one figure by the other, we see that the total number of transitions saved at $o2$ is 50%.

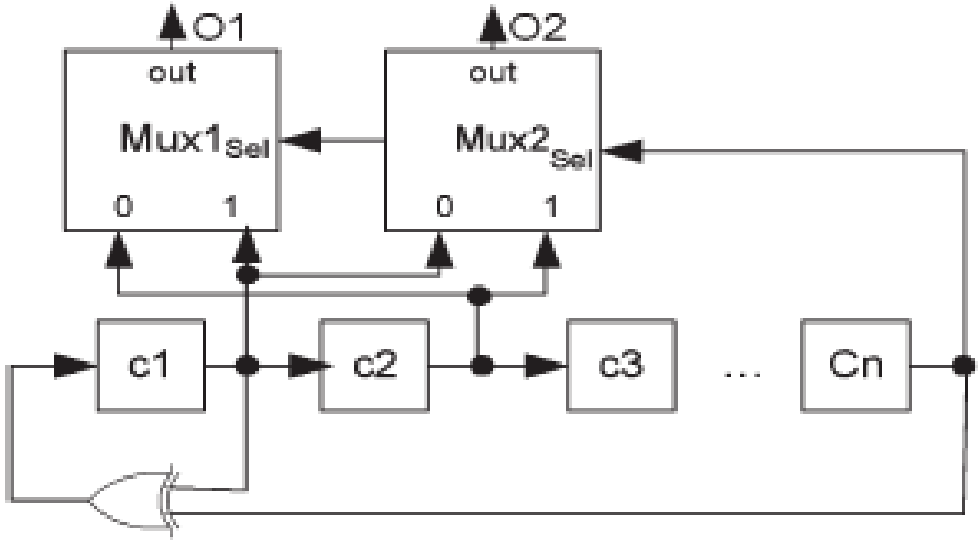

Fig2: External LFSR that implements proposed swapping arrangement.

PROPOSED:

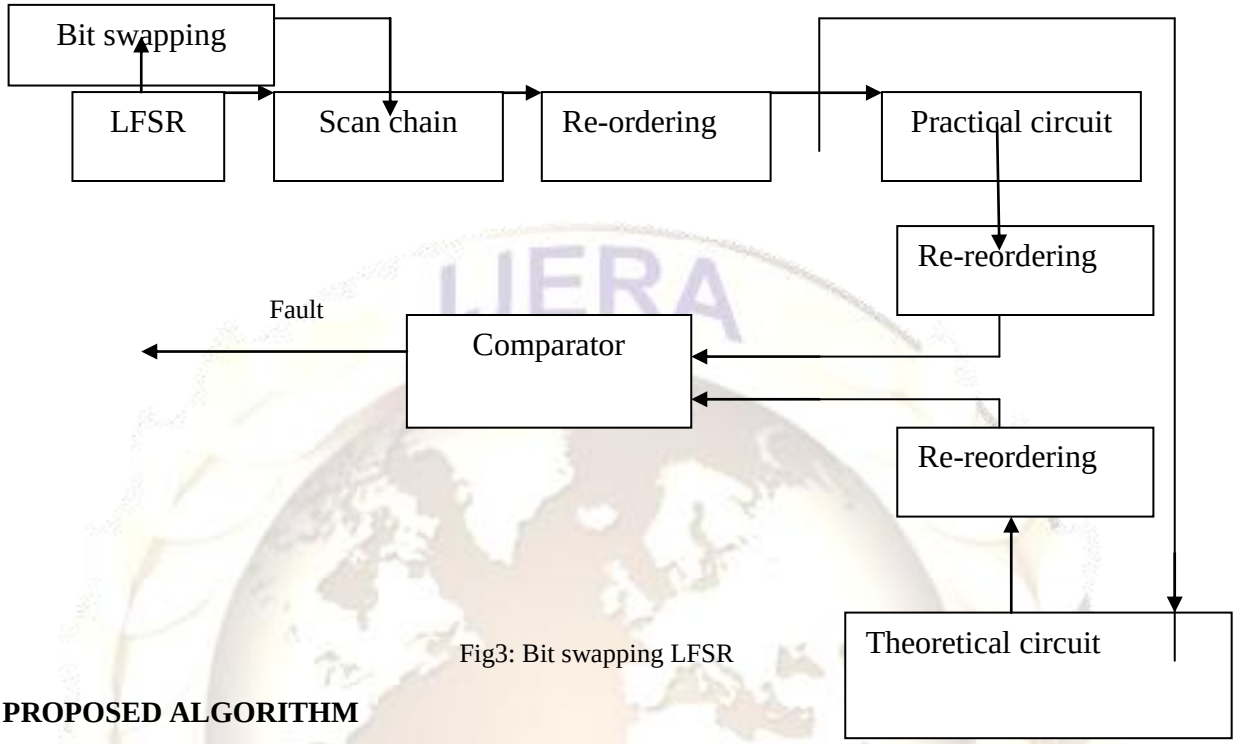

Fig3: Bit swapping LFSR

5. PROPOSED ALGORITHM

Step1: Send/make control signal so that the DUT of BIST route created and along with

Disconnect the DUT from practical use and send Busy signal to the external world.

Step 2: Place one defined set of pattern on the DUT to test.

Step 3: Get the output pattern.

Step 4: Compare the output pattern with the expected result.

Step 5: If output is OK discarding the remaining step and connect DUT for normal use.

Step 6: If result is faulty, than it state that DUT is faulty.

Step7: Discard DUT and replaced by Spare Unit and get desire output pattern.

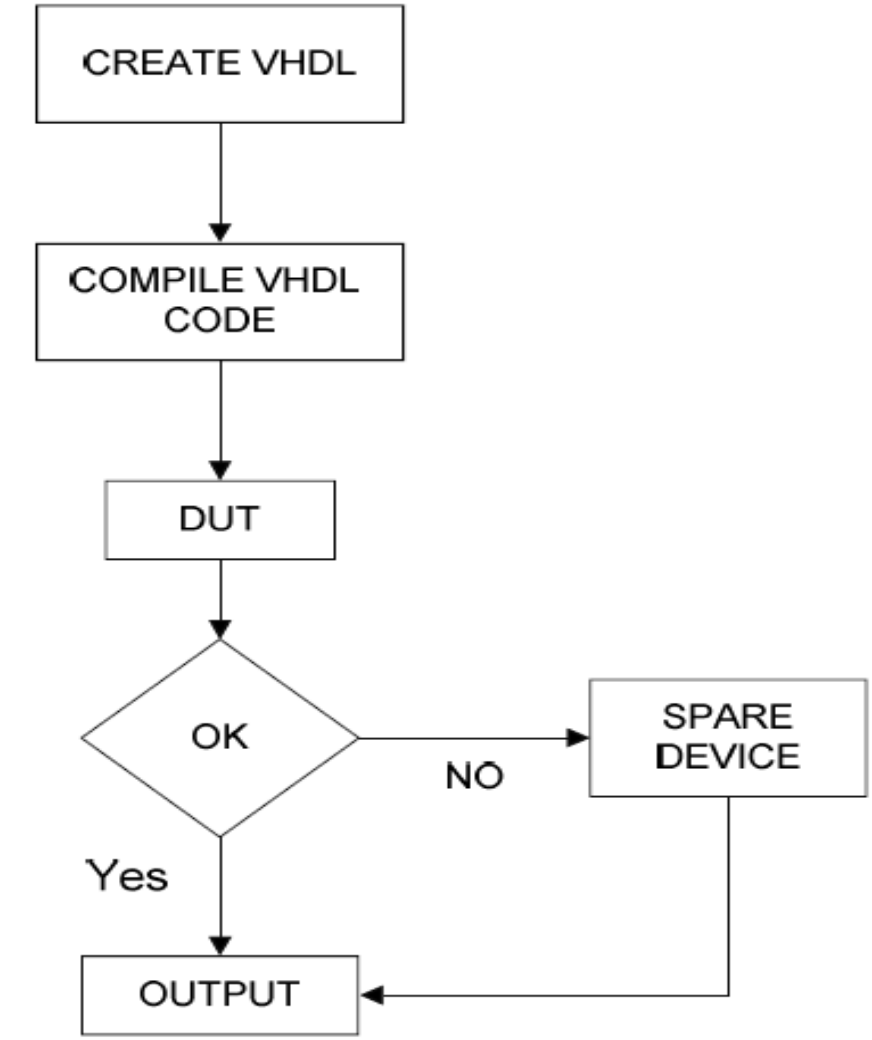

Fig: Flowchart

POSSIBLE AND SUBSEQUENT STATES FOR CELLS *c*1, *c*2, AND *cn*

LFSR OUTPUTS OF m,m+1									**Multiplexers outputs o1,o2**						
States			**Next states**			**Transition**			**States**		**Next states**		**Transition**		
C1	C2	*Cn*	C1	C2	*cn*	C1	C2	∑	O1	O2	O1	O2	O1	O2	∑
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
			0	0	1	0	0	0			0	0	0	0	0

0	0	1	1	0	0	1	0	1	0	0	0	1	0	1	1
			1	0	1	1	0	1			1	0	1	0	1
0	1	0	0	0	0	0	1	1	1	0	0	0	1	0	1
			0	0	1	0	1	1			0	0	1	0	1
0	1	1	1	0	0	1	1	2	0	1	0	1	0	0	0
			1	0	1	1	1	2			1	0	1	1	2
1	0	0	1	1	0	0	1	1	0	1	1	1	1	0	1
			1	1	1	0	1	1			1	1	1	0	1
1	0	1	0	1	0	1	1	2	1	0	1	0	0	0	0
			0	1	1	1	1	2			0	1	1	1	2
1	1	0	1	1	0	0	0	0	1	1	1	1	0	0	0
			1	1	1	0	0	0			1	1	0	0	0
1	1	1	0	1	0	1	0	1	1	1	1	0	0	1	1
			0	1	1	1	0	1			0	1	1	0	1
Transitions						8	8	16					8	4	12

6. CONCLUSION

A low-transition TPG that is based on some observations about transition counts at the output squence of LFSRs has been presented. The proposed TPG is used to generate test vectors for test-per scan BISTs in order to reduce the switching activity while scanning test vectors into the scan chain. Furthermore, a novel algorithm for scan-chain ordering has been presented. When the BS-LFSR is used together with the proposed scan-chain-ordering algorithm, the average and peak powers are substantially reduced. The effect of the proposed design in the fault coverage, test-application time, and hardware area overhead is negligible. Comparisons between the proposed design and other previously published methods show that the proposed design can achieve better results for most benchmark circuits.

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7. SIMULATION

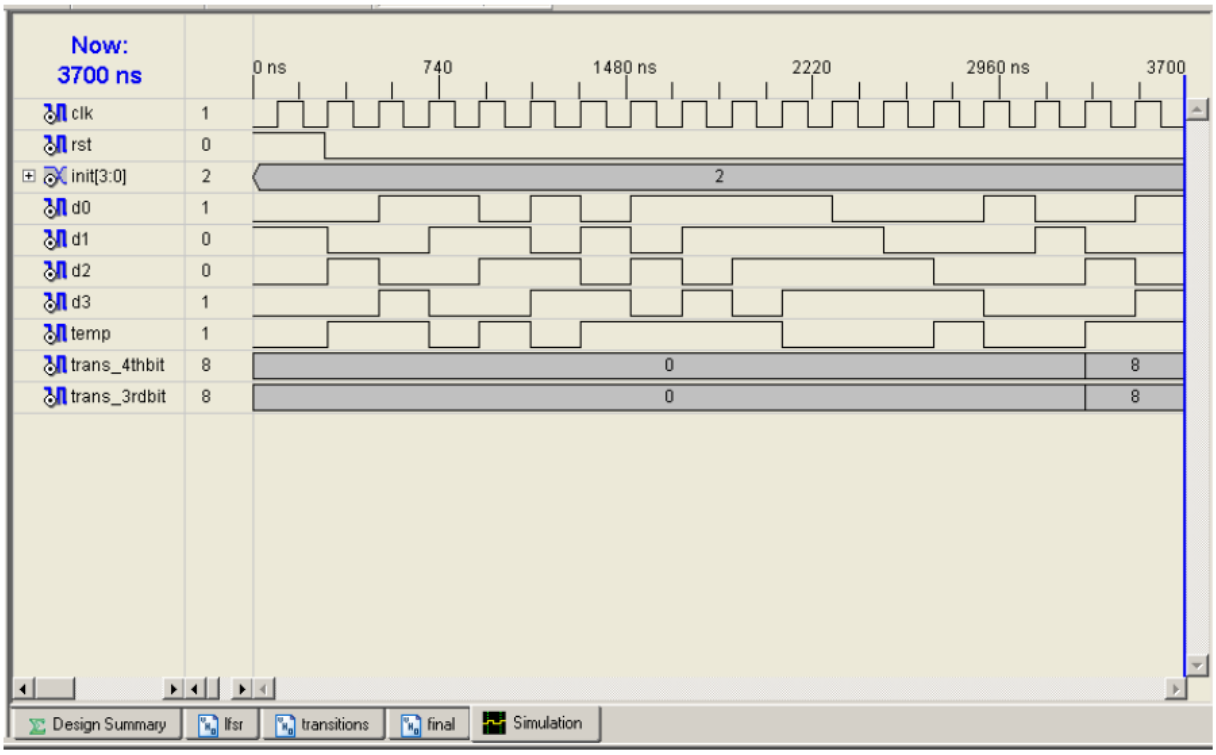

FIGURE 4.SIMULATION RESULTS WITH NORMAL LFSR

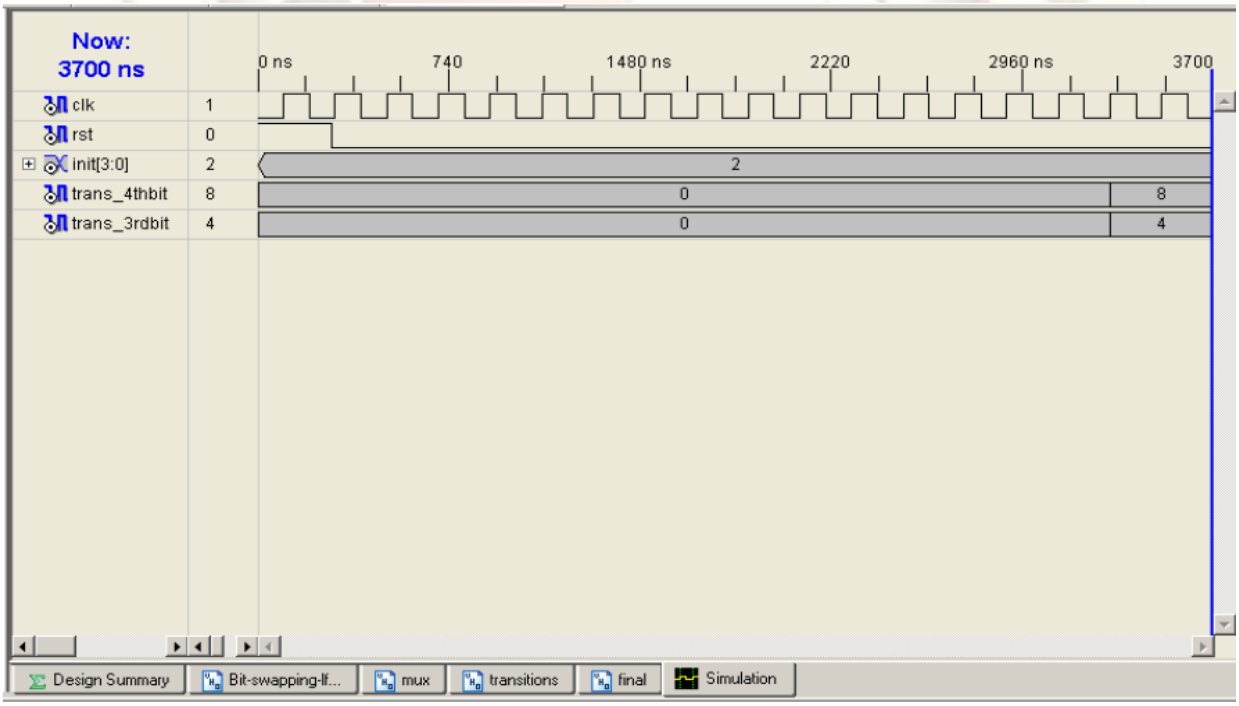

FIGURE5: SIMULATION RESULTS WITH BITSWAPPING

REFERNCES

[1] P. H. Bardell, W. H. McAnney, and J. Savir, Built-in Test for VLSI:Pseudorandom Techniques. New York: Wiley, 1997.

[2] P. Girard, "Survey of low-power testing of VLSI circuits," IEEE Des. Test Comput., vol. 19, no. 3, pp. 80–90, May/Jun. 2002.

[3] K. M. Butler, J. Saxena, T. Fryars, G. Hetherington, A. Jain, and J. Lewis, "Minimizing power consumption in scan testing: Pattern generation and DFT techniques," in Proc. Int. Test Conf., 2004, pp. 355–364.

[4] J. Saxena, K. Butler, and L. Whetsel, "An analysis of power reductiontechniques in scan testing," in Proc. Int. Test Conf., 2001, pp. 670–677.

[5] VHDL primer by J.Bhasker.

[6] A. J. Yu and G. G. F. Lemieux. Defect tolerant fpga switch block and connection block with fine grain redundancy for yield enhancement. In IEEE International Conference on Field Programmable Logic and Applications, 2005.

[7] S. Mitra, P. Sirvani, and E. McCluskey. Fault location in fpga based reconfigurable systems. In IEEE Intl High Level Design Validation and Test Workshop, 1998.

[8] W. J. Huang and E. McCluskey. Column based pre-compiled configuration technique for fpga fault tolerance. In FPGA, 2001

[9] N.Z. Haron, M.M. Ibrahim, S.A.M. Junos and Aziz. FPGA Implementation of microcode-based and FSM-based Memory built in Self Test Controllers.

[10] F. Hanchek and S. Dutt. Methodologoies for Tolerating Cell and Interconnect Faults in FPGAs. IEEE Transactions on Computers, 47(1):15–32, Jan. 1998.

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