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Modeling and Estimation of Total Leakage Current in Nano-scaled 7T SRAM Cell Considering the Effect of Parameter Variation

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ABSTRACT

In this paper we have modeled and estimated the gate leakage , the sub threshold, and the total leakage in nano scaled 7T SRAM cell by considering variation in process parameters like transistor width, oxide thickness. We have verified the results using an NMOS device of 45nm effective length and analyzed the results to enumerate the effect of different process parameters on the individual components and the total leakage. The identification and modeling of different leakage components is very important for estimation and reduction of leakage power, especially for low-power applications. This research evaluates various leakage components with parameter variation effects in 7T SRAM cell at the 45nm technology node using Cadence tool with 0.7 supply voltage . The primary contribution of this work is to estimate and modeled gate leakage, sub threshold leakage and total leakage of 7T SRAM cell by considering the effects of parameter variation.

Keywords: **7T SRAM cell, Gate Leakage, sub threshold Leakage, parameter variation,low power,**

I. INTRODUCTION

High leakage current in deep-sub micrometer regimes is becoming a significant contributor to power dissipation of CMOS circuits as threshold voltage, channel length, and gate oxide thickness are reduced.CMOS devices have been scaled down aggressively in each technology generations to achieve higher integration density and performance. With the continuing trend of technology scaling, leakage power has become a main contributor to power consumption. Moreover, the increasing statistical variation in the process parameters has emerged as a serious problem in the nano-scaled circuit design [4] and can cause significant increase in the transistor leakage current [5]-[6].Designing with the worst case leakage may cause excessive guard banding, resulting in a lower performance [5]-[6]. Hence, accurate estimation of the total leakage current considering the effect of random variations in the process parameters is extremely important for designing CMOS circuits in the nano-meter regime .By process variability of transistor mismatch becomes a major limitation of overall performance of low-voltage SRAM in nanometer CMOS process. Different leakage mechanisms contribute to the total leakage in a device the two major ones we calculated can be identified as: Sub threshold leakage, Gate leakage. Each component depends differently on the transistor geometry (gate length (Lg), oxide thickness (Tox), and width (W)), Hence, variation in each of these parameters results in a large variation in each of the leakage components, thereby, causing significant increase in the overall leakage. In this work, We have analyzed and modeled the leakage components with respect to different process parameters.

II.DESIGN OF SEVEN TRANSISTOR(7T) SRAM CELL

Fig. 1 shows the cell schematic of a 7TSRAMcell design. the cell consist of 7 transistor-2 PMOS and 5 NMOS. It consists of a cross-coupled inverter pair known as active transistor , that does data storage and There are two transistors which are known as pass transistors to load/retrieve data on bit lines, BL and BLB. .There are two word lines which are used for read and write operation. The read and write operations are controlled by the last transistor which is the most important transistor for the whole circuit operation. During a write operation, the data is loaded on the bit lines and the word select signal WS is turned high. A successful write operation occurs if the data is correctly latched in the cell. The bit lines are pre-charged to the supply voltage and the word select line is turned high to retrieve data during a read operation. A read failure can occur if the voltage drop rises higher than the threshold voltage of the cross coupled inverter pair.

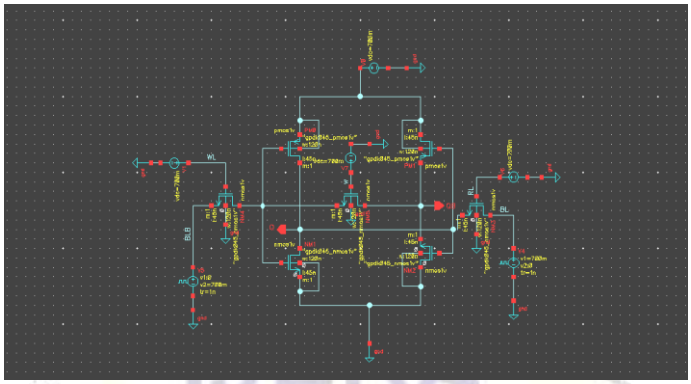


Fig2: Schematic of 7T SRAM Cell in 45 nm technology.

III. LEAKAGE COMPONENTS

The leakage current of a deep submicron CMOS transistor consists of three major components: junction tunneling current, sub threshold current, and gate tunneling current . In the following, each of these three factors is briefly discussed.

1. Junction Tunneling Leakage

The reversed biased p-n junction leakage has two main components: one is minority carriers' diffusion near the edge of the depletion region and the other is due to electron-hole pair generation in the depletion region of the reverse biased junction The junction tunneling current is an exponential function of junction doping and reverse bias voltage across the junction. Since junction tunneling current is a minimal contributor to the total leakage current , in this paper we do not attempt to measure this component of leakage in an SRAM.

2. Sub threshold Leakage

Sub threshold leakage is the drain-source current of a transistor when the gate-source voltage is less than the threshold voltage. More precisely, sub threshold leakage happens when the transistor is operating in the weak inversion region. The sub threshold current depends exponentially on threshold voltage, which results in large sub threshold current in short channel devices.

3. Gate Tunneling Leakage

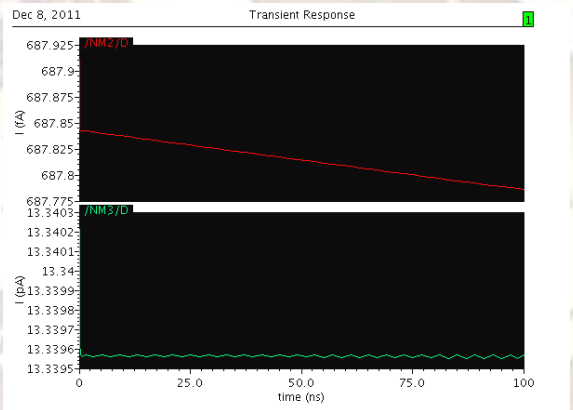
Gate leakage is the oxide tunneling current due to the low oxide thickness and the high electric field which increases the possibility that carriers tunnel through the gate oxide.Gate tunneling current is composed of three major components: (1) gate to source and gate to drain overlap current, (2) gate to channel current, part of which goes to source and the rest goes to drain, and (3) gate to substrate current.

IV. ESTIMATION OF LEAKAGE COMPONENTS

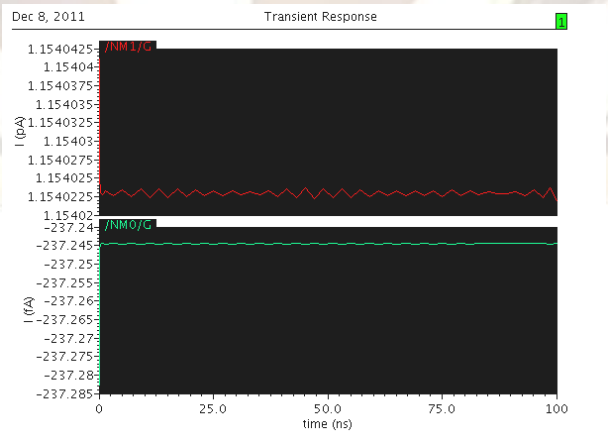
In the "off" state of a transistor the major leakage components are: the gate leakage and the sub threshold leakage (Isub) In this section we modeled and estimate the three leakage components considering variation in the transistor geometry (Lg,, Tox, W). Each of the parameters is considered to being dependent of each other .The model is derived considering an NMOS device of 45nm effective length at room temperature (T=27°C). The nominal values of the parameters are chosen based on the models available in Cadence tool. We vary the width and oxide thickness and then estimate and modeled the effects of these variations. For each leakage component the analytical models are verified on spectre simulations which is available on Cadence Tool.

TABLE shows the measurements of gate leakage,subthreshold leakage and total leakage

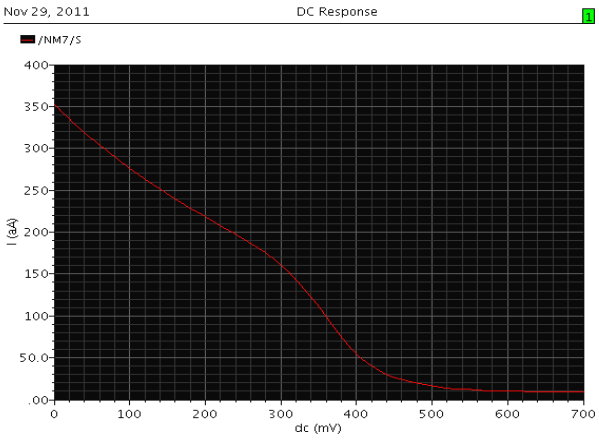
Parameters	Without Process variation effects	With Process variation effects
Gate Leakage	-24.9755fA 62.782fA	-237.2443fA 1.154022pA
Sub threshold leakage	2.685 µA 1.145nA	687.78fA 13.33957pA
Total Leakage	8.0961aA	9.7976aA



(a)



(b)



(c)

Figure 4.1: Distribution of leakage components with the Simultaneous variation on parameters. (a) Gate leakage , (b) Suthreshold leakage , and (c) Total Leakage

V. CONCLUSION

In this paper we have designed a 7T SRAM cell for optimizing the power and performance with process variation in 45 nm technology mode using the cadence tool .In this research we modeled and estimated the effect of the parameter variation on the gate, the sub threshold, and the total leakage. The models have been verified with Spectre simulations. Due to the exponential relation of leakage current with process parameters, such as the effective gate length, oxide thickness and doping concentration, process variations can cause a significant increase in the leakage current and power. It has been shown that the parameter variation has significant impact on each leakage component and can cause large variation in the total leakage. Hence, in conclusion we believe that, the derived model will be extremely useful in the estimation of the total leakage in logic circuits considering the effect of parameter variations.

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